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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 10/602,195 | 06/24/2003 | Melvin W. Stene | 14993.29 | 9997 |

22913 7590 03/02/2007

WORKMAN NYDEGGER
(F/K/A WORKMAN NYDEGGER & SEELEY)
60 EAST SOUTH TEMPLE
1000 EAGLE GATE TOWER
SALT LAKE CITY, UT 84111

| EXAMINER | |
|---|---|
| GHEBRETINSAE, TEMESGHEN | |
| **ART UNIT** | **PAPER NUMBER** |
| 2611 | |

| SHORTENED STATUTORY PERIOD OF RESPONSE | MAIL DATE | DELIVERY MODE |
|---|---|---|
| 3 MONTHS | 03/02/2007 | PAPER |

**Please find below and/or attached an Office communication concerning this application or proceeding.**

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/602,195 | STENE, MELVIN W. | |
| | Examiner | Art Unit | |
| | Temesghen Ghebretinsae | 2611 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-17 and 20-28* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *1-17* is/are allowed.

6)☒ Claim(s) *20-28* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *6/24/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

## DETAILED ACTION

1. It would be of great assistance to the Office if all incoming papers pertaining to a filed application carried the following items:

1. Application number (checked for accuracy, including series code and serial no.).
2. Group art unit number (copied from most recent Office communication).
3. Filing date.
4. Name of the examiner who prepared the most recent Office action.
5. Title of invention.
6. Confirmation number (See MPEP § 503).

### *Information Disclosure Statement*

2. The IDS filed 6/24/03 has been consider by the examiner.

### *Claim Objections*

3. Claim 1 is objected to because of the following informalities: in claim 1, line 8, and claim 14, line 2 "the output terminal" should be ---an output terminal---. Appropriate correction is required.

### *Claim Rejections - 35 USC § 112*

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Claim 28 rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claim 28, line 9, and line 20, "the control" and "the control circuit" should be ---the phase detector---. (See claim 20).

### *Claim Rejections - 35 USC § 102*

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

7. Claims 20-28 are rejected under 35 U.S.C. 102(b) as being anticipated by Waldrop (6,452,431).

Consider claims 20-28 as claimed now. Waldrop discloses a delay locked loop circuit (101) comprising: a delay line configured to receive a clock signal and pass the clock signal through an adjustable number of delays elements (102,113); a phase detector (116) configured to compare a phase of clock signal at an output terminal of the delay line and received at a feedback clock input of the phase detector and the clock signal received at a reference input of the phase detector, and configured to generate a fist signal (118) when the phase of the clock signal at the feedback circuit input of the phase detector is not approximately equal to the phase of the reference clock signal at a reference input of the phase detector; the phase detector is further configured to generate a second signal (120) when the phase of the feedback clock input of the phase detector is not approximately equal to the phase of the reference clock signal at a reference input of the phase detector; a filter (108) configured to perform the following: receiving the first signal from the phase detector(receiving a second signal from the phase detector); determining whether the reception of the first signal,(118) (second signal 120) results in a predetermined number of consecutive first signals received from the phase detector and adjusting the adjustable number of delay

elements (or not adjusting the number of delay elements when clock signals are substantially synchronized). (See fig.1 and col.2, line 31 to col.3, line 36. The first predetermined number is the same as the second predetermined number as claimed in claim 22; and the predetermined number is more than one or more than two or eight (105A-105N) as claimed in claims 24-26.

8. Claims 20 and 28 are rejected under 35 U.S.C. 102(b) as being anticipated by Millar (6,337,590)

9. Consider claims 20 and 28 as claimed now. Millar discloses a delay locked loop circuit (fig.3) comprising: a delay line configured to receive a clock signal and pass the clock signal through an adjustable number of delays elements (13,17); a phase detector (25) configured to compare a phase of clock signal at an output terminal of the delay line and received at a feedback clock input of the phase detector and the clock signal received at a reference input of the phase detector, and configured to generate a fist signal (UP) when the phase of the clock signal at the feedback circuit input of the phase detector is not approximately equal to the phase of the reference clock signal at a reference input of the phase detector; the phase detector is further configured to generate a second signal (DOWN) when the phase of the feedback clock input of the phase detector is not approximately equal to the phase of the reference clock signal at a reference input of the phase detector; a filter (29,31) configured to perform the following: receiving the first signal from the phase detector(receiving a second signal from the phase detector); determining whether the reception of the first signal(UP) (second signal DOWN) results in a predetermined number of consecutive first signals received from the

phase detector and adjusting the adjustable number of delay elements (or not adjusting the number of delay elements when clock signals are substantially synchronized). (See fig.3 col.5, lines 15-32 and fig.5, col.5, line 42 to col.6, line 57)

> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

10. Claims 20-28 are rejected under 35 U.S.C. 102(e) as being anticipated by Bell et al (US2003/0215040).

Consider claims 20-28 as claimed now. Bell discloses a delay locked loop circuit (100) comprising: a delay line configured to receive a clock signal and pass the clock signal through an adjustable number of delays elements (302.1,302.n;115.1,115.n); a phase detector (304) configured to compare a phase of clock signal at an output terminal of the delay line and received at a feedback clock input of the phase detector and the clock signal received at a reference input of the phase detector, and configured to generate a fist signal (SL) when the phase of the clock signal at the feedback circuit input of the phase detector is not approximately equal to the phase of the reference clock signal at a reference input of the phase detector; the phase detector is further configured to generate a second signal (SR) when the phase of the feedback clock input of the phase detector is not approximately equal to the phase of the reference clock signal at a reference input of the phase detector; a filter (306) configured to perform the following: receiving the first signal (SL) from the phase detector(receiving a second signal(SR) from the phase detector); determining whether the reception of the

first signal,(SL) (second signal SR) results in a predetermined number of consecutive first signals received from the phase detector and adjusting the adjustable number of delay elements (or not adjusting the number of delay elements when clock signals are substantially synchronized). (See fig.3 paragraph {0030-0035}. The first predetermined number is the same as the second predetermined number as claimed in claim 22; and the predetermined number is more than one or more than two or eight (115.1,115.n;302.1,302.n) as claimed in claims 24-26.

***Allowable Subject Matter***

11. Claims 1-17 are allowed.

12. The following is a statement of reasons for the indication of allowable subject matter: the prior art of record fail to anticipate or render obvious the claimed method for generating a fixed angle delayed clock signal as compared to a reference clock signal while compensating for skew introduced by system clock delay, the method comprising the following steps:
passing a reference clock signal through a reference clock delay line comprising a plurality of reference clock delay elements; adjusting a number of reference clock delay elements through which the reference clock signal passes in the reference clock delay line until the reference clock signal at the output terminal of the reference clock delay line and received at a feedback clock input of a phase detector and the reference clock signal received at a reference input terminal of the phase detector are approximately in phase; calculating an initial number of fixed angle clock delay elements in a fixed angle clock delay line needed to generate a fixed angle delayed clock signal with respect to the reference clock signal, the calculation being based on the number of reference clock delay elements used at the time the reference clock signal at the reference input of the phase detector and the reference clock signal at the feedback clock input of the phase detector are approximately in phase; receiving a clock signal from the fixed angle clock delay line; passing the clock signal through a system clock mechanism that introduces

the system clock delay; calculating an adjustment number of fixed angle clock delay elements needed to account for the system clock delay using the clock signal received from the fixed angle clock delay line and the clock signal after having passed through the system clock mechanism; calculating a final number of fixed angle clock delay elements needed to generate a fixed angle delayed clock signal that accounts for the system clock delay by adjusting the initial number of fixed angle clock delay elements by the adjustment number of fixed angle clock delay elements; receiving the reference clock signal at an input terminal of the fixed angle clock delay line; and
passing the reference clock signal through the final number of fixed angle clock delay elements before allowing the reference clock signal to be output from the fixed angle clock delay line in the form of the fixed angle delayed clock signal that accounts for system clock delay as claimed in claims 1 and 17.

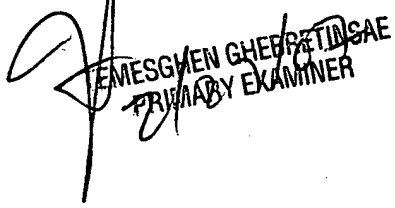
13. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Temesghen Ghebretinsae whose telephone number is 571-272-3017. The examiner can normally be reached on Monday-Friday from 8 to 6. The examiner can also be reached on alternate .

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jay Patel, can be reached on 571-272-2988. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should

you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Temesghen Ghebretinsae
Primary Examiner
Art Unit 2611




T.Ghebretinsae

2/26/07.